VMMK-xxxx
Assembly, Cleaning and Handling

Application Note 5378

Introduction

The purpose of this application note is to provide an introduction to the package style of the VMMK products and to discuss SMT techniques for assembly. With the rapidly changing techniques in the SMT area, it is expected that this application note will be continually updated as new processes have been proven by both Avago and our customers.

Description

Avago Technologies has combined our industry leading E-pHEMT technology with a revolutionary wafer level chip scale package design (WLCSP) using a Wafer-Cap process. This wafer level chip scale package is shown next to a typical 0402 capacitor for comparison in Figure 1. The 0402 capacitor is on the right, and the 1 mm x 0.5 mm WLCSP is on the left. This WLCSP is attractive compared to other packaging in terms of cost and size. Tape and reel capability is standard for chip shooter pick and place applications.

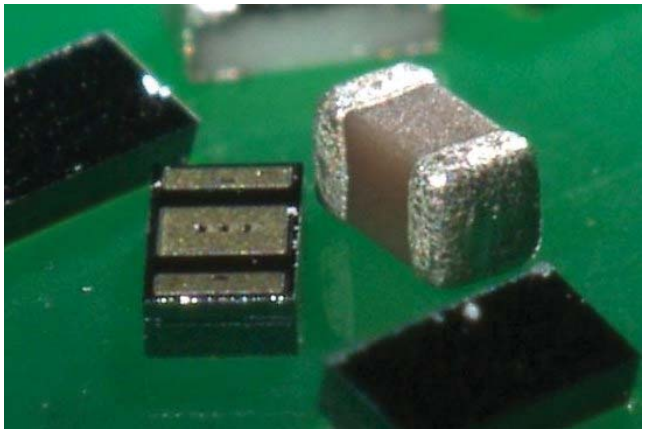

Figure 1. VMMK device is half the height of a standard 0402 capacitor.

Package Construction

This package is a non-hermetic wafer level chip scale package which contains a cavity and comprises a Gallium Arsenide top cover (Cap) and a bottom Gallium Arsenide substrate (base), as shown in Figure 3 and Table 2. Active circuitry is on the base and is internal to the cavity. A gasket is used to bond the cap to the base at the perimeter of the die. The gasket is comprised of BCB polymer manufactured by Dow Chemical. This construction should be a consideration for handling and shear testing.

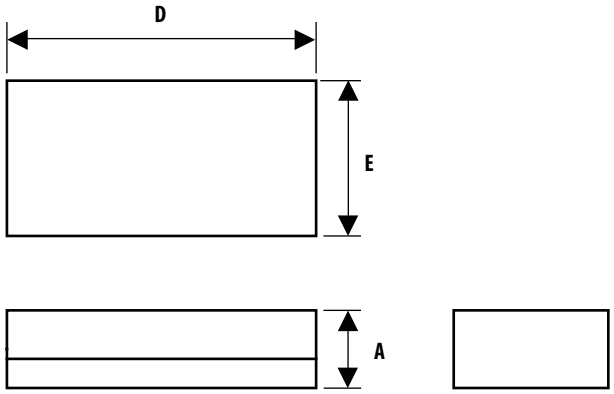

Figure 2. Outline drawing of VMMK Wafer-Cap device

Table 1. VMMK package dimensions

Dimension	Min (mm)	Max (mm)
A	0.225	0.275
D	1.004	1.085
E	0.500	0.585

SMT Assembly Process

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating, circuit board material, conductor thickness, pattern, type of solder paste and solder alloy, thermal conductivity, and thermal loading and mass of components. Chip scale components such as this device will reach solder reflow temperatures faster than those with a greater mass. Reflow temperature settings need to be determined by the end user based on these considerations. Also, moisture sensitivity MSL level 2 has been qualified for this device. The MSL level 2 conditions must not be exceeded.

Table 2. Wafer-Cap thickness dimensions

Top cover (Cap) Final Thickness	140 µm
Gasket Thickness	10 µm
Substrate (Base) Final Thickness	100 µm
Total Package Thickness	250 µm

Device Footprint

This device is similar to the standard 0402 capacitor form factor, but does not use a standard 0402 land pattern. The device backside metal pattern is comprised of three solder pads as depicted in the bottom view shown in Figure 4. Pin 1 is identified by an opening in the metal at the corner of the input pad which is designated port 1. This figure shows the metal pad footprint dimensions for the solder process. Dimensions are in mm. A solder resist layer (solder stop) surrounds the pads to inhibit solder bridging. The gap between the pads must not be bridged with solder. The package lead material is a minimum of 3 µm thick Au under 5000 Angstroms of a barrier diffusion layer and 3000 Angstroms Ni with 500 Angstroms of Au flash. When liquid solder is present, the Au flash dissolves and the Ni layer becomes wetted to the liquid solder. This occurs during the solder reflow process when attaching the device to the PCB.

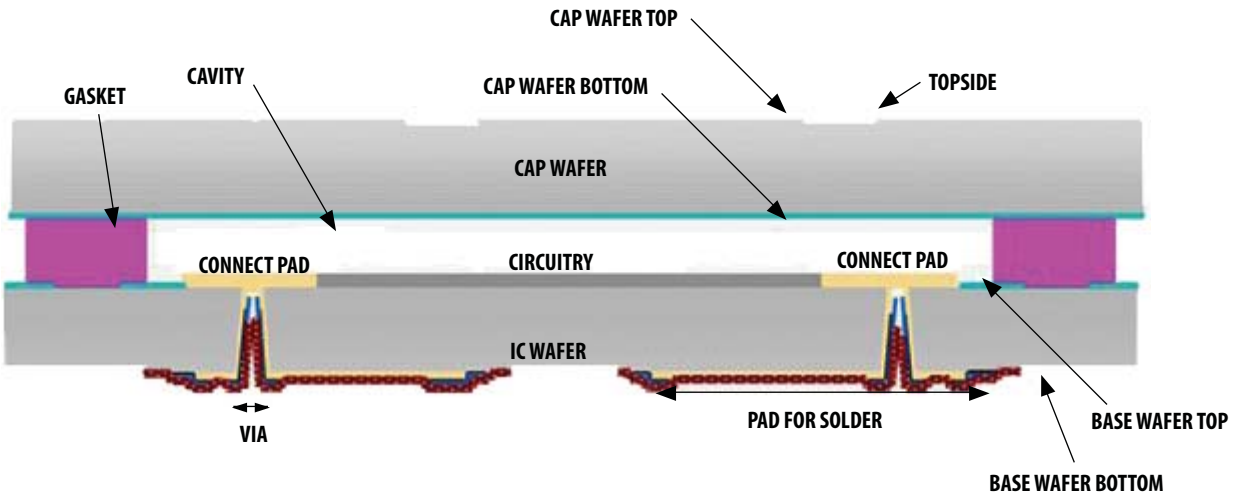

Figure 3. Cross section side view showing major elements: lid, cap, and gasket (not to scale)

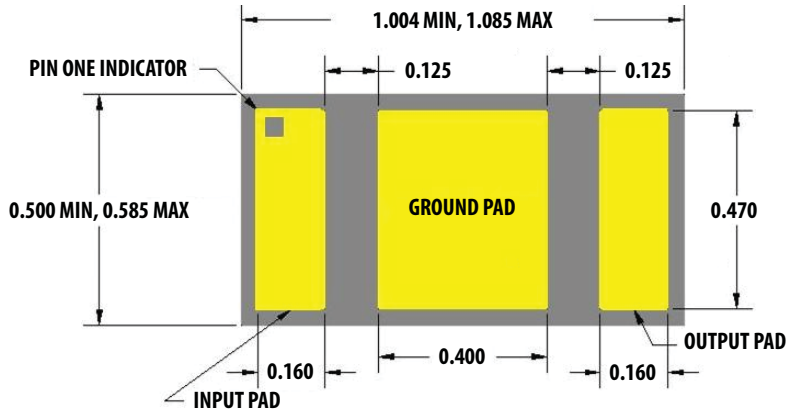

Figure 4. Solderable area of the device shown in yellow. Dimensions in mm.

Printed Circuit Board Material and VIAs

The PCB board material stack used to qualify the device consists of 40 mil thickness FR4 core material with one ounce copper for both top and bottom metal. Soldering onto materials with greater thermal expansion than FR5 or high Tg FR4 should be avoided. Board materials with high CTE, such as Teflon, may lead to damage of the base of the GaAs package which contains the device circuitry or may lead to damage of the cap of the GaAs package which defines the air cavity, or may lead to damaging both. Low loss microwave materials such as RO4003 and RO4350 have CTEs similar to FR4 type material and should be acceptable PCB materials.

Recommended PCB Footprint and Grounding

Establishing a proper ground for either the source leads of the VMMK-1XXX series or the common leads of the VMMK-2XXX and -3XXX series is paramount. The recommended printed circuit board VIA pattern is shown in Figure 5. This is a non-solder mask defined footprint (NSMD). The outline of the solder mask that borders the device is shown by the area indicated in green.

The recommended footprint does not require any plated through holes under the device. Modeling and tests indicate that placing VIAs adjacent to (within .003") and on either side of the device as shown in Figure 5 provides good grounding for the VMMK-2XXX and VMMK-3XXX series devices when mounted on .010" thickness RO4350 printed circuit board material. This technique also applies when using the VMMK-1XXX discrete FETs at frequencies greater than 10 GHz. When using the VMMK-1XXX FETs at low frequencies, some amount of source inductance may actually be required. In this case, the VIAS may be placed further away from the device to enhance stability. Consult individual application notes for more information.

Due to the proximity of the VIAs to the edge of the VMMK device (less than .003 "), it is recommended that the VIAs be filled to minimize wicking of the solder from under the VMMK device. In addition, since the edge of the VIAs is slightly outside of the solder mask area, the VIAs should be filled.

VIAS can be filled with a conductive VIA fill material or a non-conductive VIA fill material. Possible non-conductive VIA fill materials include:

San-Ei Kagaku PHP-900 IR6
Taiyo Ink HB 12000 DB4
Dielectric prepreg material
Solder mask material

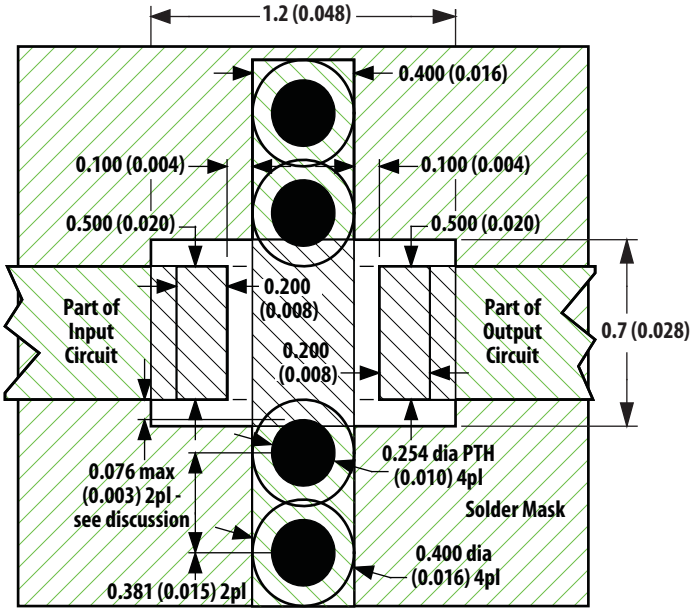

Figure 5. Recommended PCB layout for VMMK devices

As a general rule, if a VIA is within .004" (100u) of the edge of the soldermask but not under the device, then the VIA should be filled. Any VIA which is covered by the solder mask and is beyond .004" (100u) of the solder mask edge can be uncapped and unfilled as it is not at risk of wicking away solder from the device.

If for any reason it is required to include a VIA or VIAs under a VMMK device, then the VIAs should be filled and capped. A capped VIA is a "plated over" filled VIA. If a filled but uncapped VIA is placed under the device, there will not be enough solderable surface area for device attachment. If an unfilled and uncapped VIA is placed directly under the ground pad, then the liquid solder will flow into the open VIA hole during the reflow process and deplete the solder volume to varying degrees from under the ground pad. Depletion of the solder volume due to unfilled VIAs may lead to a weak solder joint, poor grounding of the device, and/or stresses compromising the structural integrity of the package.

The recommended footprint provides a solder joint that meets JEDEC standards for die shear, and provides sufficient adhesion of the ground lead such that the mechanical integrity of the package remains intact should any minor deformation of the board occur due to thermal shock.

Recommended Solder material and PCB Finish

Several different solder pastes are suggested, but not required. Solder pastes that include no-clean or water soluble flux are preferred. These have been evaluated and are suitable for SMT assembly of this device:

- Alpha Metals solder paste WS820, Water Soluble, type 3, SAC305, lead-free 96.5 Sn/3.0 Ag/0.5 Cu. This composition has a melting point of 217-219°C.
- Indium solder paste 3.2, Water Soluble, type 4, SAC305 lead-free 96.5 Sn/3.0 Ag/0.5 Cu
- RX303-92SKHO manufactured by Nihon Handa, solder composition Sn96.5 Ag3.5 and a melting point of 218-220°C

The following PCB surface finishes were evaluated to be suitable for this device.

- OSP surface finish
- ENIG surface finish

Recommended Chip Shooters

The following chip shooters have been evaluated to be suitable for this device. These were used with standard settings and nozzles:

- Zuki Model KE-2050RL
- Panasonic MSF NM-MD15

Solder stencil design

The stencil should be compatible with the PCB land pattern on figure 5. A properly designed stencil is required to ensure an optimum amount of solder paste is deposited onto the PCB pads for the assembly application. Stencil design depends on application factors such as stencil thickness, materials, and process control. The stencil pattern shown in Figure 6 was evaluated and is suggested for SMT assembly. The angled outer edges could help fill the stencil when the squeegee pass is slightly off axis.

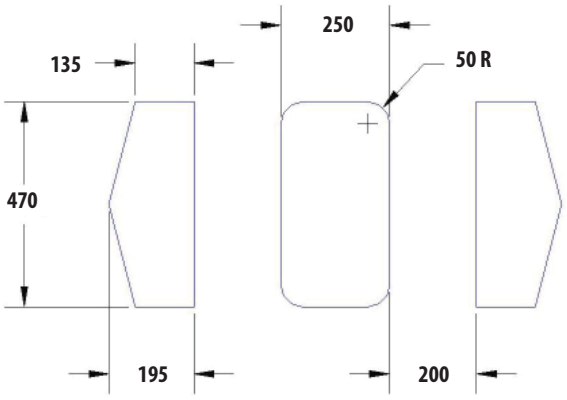

Figure 6. Recommended stencil pattern. Dimensions in microns. Stencil thickness 100 microns. Stencil type: laser cut.

Solder Reflow Process

The infrared/convection reflow profile investigated and recommended by Avago for this product is based on JEDEC/IPC standard J-STD-020 revision C. This device has been qualified to withstand a maximum of 3 cycles of solder reflow according to the conditions of J-STD-020 C. Further reflow would degrade the die metal interface with the solder. This device has not been designed or qualified for wave soldering or vapor phase reflow. These processes are not recommended.

Profile for Reflow Soldering

Figure 7 depicts the standard lead-free JEDEC/IPC profile qualified for this device. Table 3 lists the parameters and peak temperatures as indicated by JEDEC/IPC. The most recommended and most common reflow method is accomplished in a belt furnace using convection/ IR heat transfer.

This profile shows the actual temperature range that could occur on the surface of a test board at or near a central solder joint. After ramping up from room temperature, the circuit board with components held in place with solder paste, passes through a preheat zone. The preheat zone increase the temperature of the board and components to prevent thermal shock. During this type of reflow soldering, the circuit board and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs thermal energy more efficiently, and then distributes this heat to the components. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

Do not use prolonged hot preheat due to excessive oxidation which can occur on the solder powder surface. The time over 217 degrees C is critical and will determine the appearance and integrity of the solder joint after reflow. Longer reflow time may result in excessive inter-metallic growth, dull and gritty solder joint appearance, and charring of flux residues. Time below 30 seconds may result in insufficient wetting and poor intermetallic formation.

As a general guideline, this device should be exposed to only the minimum lead-free process temperature and times necessary to achieve a uniform reflow of solder on the board. The rates of change of temperature for the ramp-up and cool-down zones are specified by J-STD-020c standard to be low enough to not cause deformation of the board or damage to components due to thermal shock. This profile allows a reflow temperature which is low enough to avoid damaging the internal circuitry during solder reflow operations provided the time of exposure at peak reflow temperature is not excessive per the JEDEC standard.

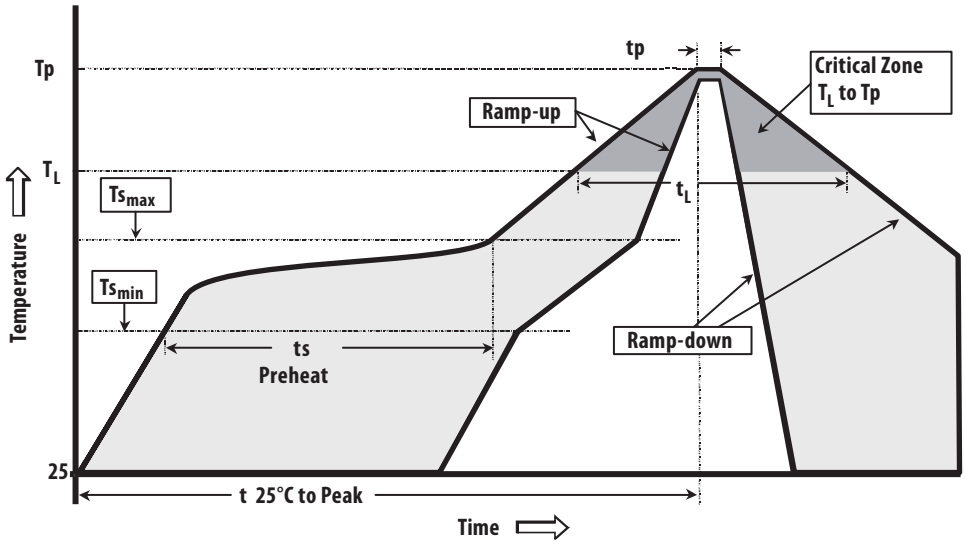

Figure 7. Standard lead-free solder reflow profile (JEDEC/IPC J-STD-020C)

Table 3. Standard lead-free solder reflow profile (JEDE/IPC J-STD-020C)

Reflow Parameter		Lead-Free Assembly
Average ramp-up rate (Liquidus Temperature) ($T_{S(max)}$ to Peak)		3° C/second max
Preheat	Temperature Min ($T_{S(min)}$)	150°C
	Temperature Max ($T_{S(max)}$)	200°C
	Time (min to max) (t_S)	60-180 sec
$T_{S(max)}$ to T_L Ramp-up Rate		3°C /sec max
Time maintained above:	Temperature (T_L)	217°C
	Time (T_L)	60-150 sec
Peak temperature (T_p)		260 +0/-5°C
Time within 5°C of actual Peak Temperature (t_p)		20-40 sec
Ramp-down Rate		6°C /sec max
Time 25°C to Peak Temperature		8 min max.

Note
1. All temperatures refer to topside of the package, measured on the package body surface.

Reference

1. JEDEC/Electronic Industries Alliance, Inc, "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices (IPC/JEDEC J-STD-020C)," July 2004.

Board cleaning

This device is suitable for standard aqueous cleaning with DI water and solvent cleaning processes. This device has not been designed for ultrasonic cleaning or vapor phase cleaning and these processes are not recommended.

The device uses BCB polymer as a gasket material to bond the top GaAs wafer to the bottom GaAs wafer, and this creates a cavity inside the device for the active region. This BCB is produced by Dow Chemical, and is the only polymer used for the device exposed to board cleaning chemicals. BCB has been used often in the semiconductor industry for die passivation. This includes applications with BCB on exposed surfaces of flip chips and wafer level chip scale packages. The customer should check the compatibility of their selected board cleaner with the cleaning chemical manufacturer. The manufacturers of board cleaning chemicals are the authoritative resource for providing specific information or evaluations to customers about their compatibility with polymers and other materials used in board assembly. Dow Chemical may provide additional nformation to customers regarding the general compatibility of BCB exposure to board cleaning. Dow technical inquiries in the USA phone 800-441-4369

System in package applications

This device has not been designed or qualified for over-molding or encapsulation. Molding pressures may impart sufficient stress to compromise the GaAs cavity and render the device non-functional.

Use of Conductive Epoxy

Conductive epoxy should not be used as an alternative to solder paste. Conductive epoxy can smear across the gap between the input, ground, and output pads, resulting in device shorts.

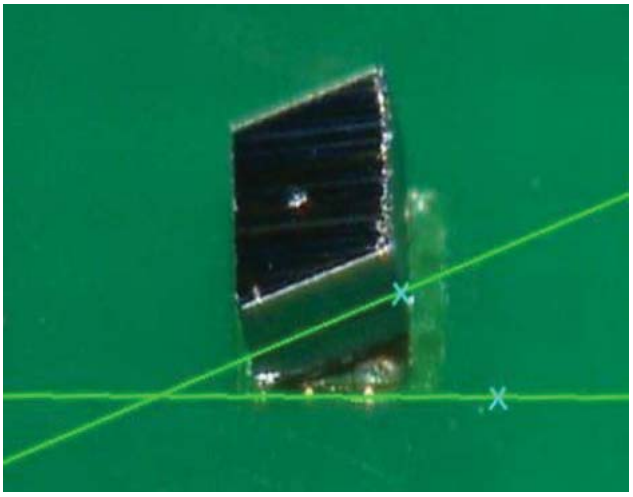

Figure 8. Soldered unit with 5 to 20 degrees of tilt on the PCB

Die Shear Testing

It is acceptable for soldered units to have some tilt as the solder reflows under the device. A photo of a soldered unit is shown in Figure 8. A tilt of 5 to 20 degrees along the long axis is typical for this device after the solder reflow process. Parts assembled with this tilt were subjected to die shear testing and passed solder qualification tests. The suggested method of applying side pressure for the die sheer testing is shown in Figure 9. Make sure that pressure is applied to both top and bottom of the device and if possible make sure that pressure is even between the top and bottom. Try to avoid a situation as shown in Figure 10. If the tilted die is sheared such that the shear tool pushes only the cap edge or makes contact with the cap without making contact with the base, it would be possible to sever the cap at the gasket, giving a false shear reading. If the shear tool is too far from the PCB surface, only the cap will be sheared. This would result in a false reading.

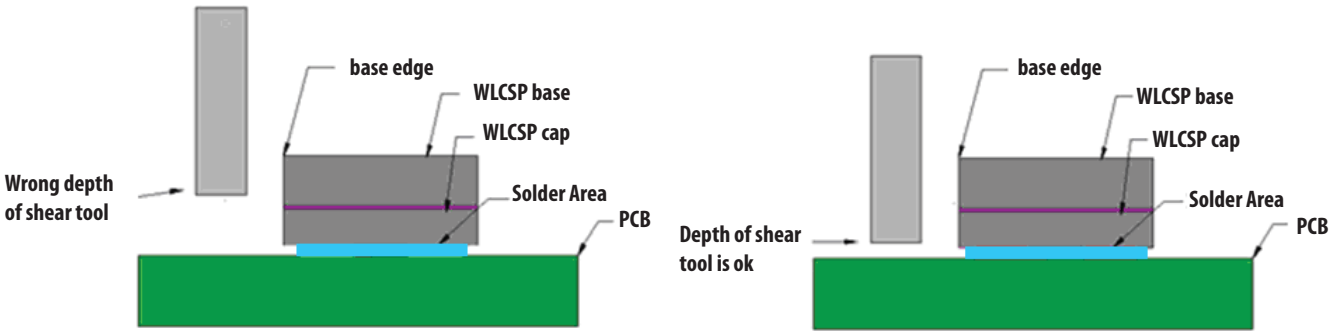

Figure 9. Die shear tool set-up showing desired (right) vs undesired (left) tool location

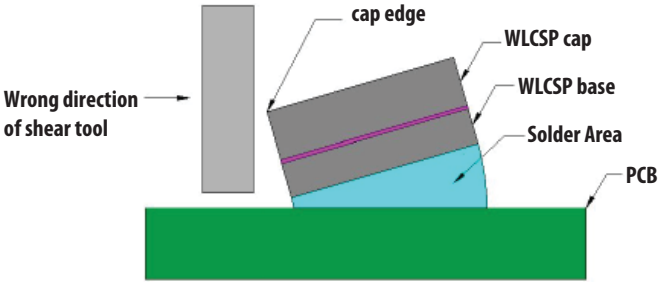

Figure 10. Avoid applying pressure directly to the top edge of the cap

Typical die shear results with lead-free solder paste are shown in Figure 11. The minimum shear value specified is 0.3 Kgf.

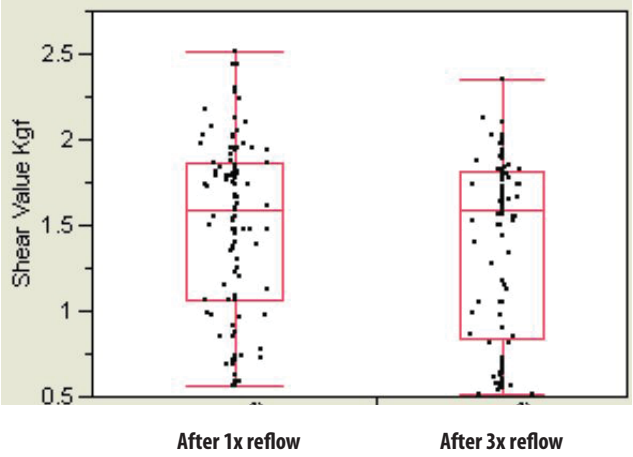

Figure 11. Typical die shear results with lead-free solder paste

ESD Sensitivity

Note: These devices are ESD sensitive. The following precautions are strongly recommended. Ensure that an ESD approved carrier is used when die are transported from one destination to another. Personal grounding is to be worn at all times when handling these devices. Additional information can be found in Avago Application Note A004-R:Electrostatic Discharge Damage and Control. Reliability information including ESD classifications for each VMMK device can be found in the individual Reliability Data Sheets.

Manual Assembly for Prototypes

Handling of the VMMK device should be along the sides when using tweezers or from the topside when using a vacuum collet.

The recommended attachment is to use a solder paste pattern as shown in Figure 12.

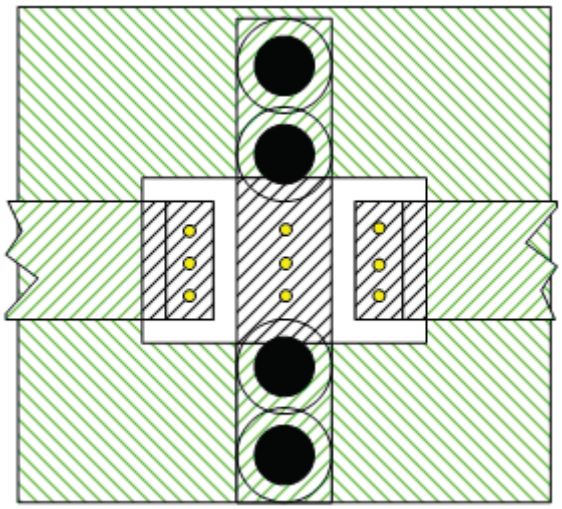

Figure 12. Solder paste pattern of 9 dots shown in yellow.

Apply solder using either a stencil printer or dot placement. The pattern for each pad consists of 3 dots of solder with an approximate diameter of 50um and about 85um high. They should be at least 50um away from the edge of the pad, otherwise shorting between pads may occur during reflow. Excessive solder can also degrade RF performance. Once the solder is in place, place the VMMK device on the solder, applying a small amount of downward pressure. Use the manufacturer's recommended solder reflow profile for the solder. A standard profile will have a steady ramp up from room temperature to the pre-heat temp to avoid damage due to thermal shock. Be sure to not exceed the maximum temperatures and times as shown in Figure 7 and table 3. Clean off flux per vendor's recommendations. Clean module with Acetone and rinse with alcohol. Allow the module to dry before testing.

Avago uses Solder Plus 96NCLR-A for prototype boards which has a melting point of 221°C.

Conductive epoxy is not recommended. Hand soldering is also not recommended.

Rework Procedure

If a VMMK device is suspected of being inoperative due to a bad solder joint, it is first suggested that the circuit board and device be reflowed without removing the device. If a solder reflow does not fix the problem, then we recommend replacing the device. This can be done manually on a hot plate or if a semi-automated rework machine is used, the forced-air collet would use a standard reflow profile as shown in Figure 7 to re-liquify the solder under the device.

When replacing a device, any existing solder on the etch should be removed as best as possible and then solder should be redeposited with a solder dispenser or needle in accordance with the solder paste pattern shown in Figure 12. If a semi-automated rework machine is used, the solder would be applied using the predefined stencil pattern as shown in Figure 6.

Summary

As new assembly information becomes available, this application note will be updated. Check www.avagotech.com for periodic updates.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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